Amendments To The Specification

Please amend paragraph 0028 as follows:

[0028] So configured, the differential amplifier 701 includes the capability of using the error correction parameter to provide an output comprising a resultant error-corrected signal (and preferably an output signal that is also amplified by a gain and wherein common mode noise has been substantially deleted therefrom). As will also be shown below in more detail, this configuration can also be utilized to ensure that the differential amplifier 701 output signal includes a predetermined offset 703 (to lift, for example, the resultant signal to a desired position within a given operating range of values).

Please amend paragraph 0030 as follows:

[0030] FIG. 6 depicts a conceptual diagram of a preferred embodiment. An input signal composed of undesired common mode [[1]] 60, DC offset [[2]] 62, undesired low frequency signals [[10]] 63, and a desired differential AC signal is presented to differential high pass filter [[5]] 64. As noted above, the signal of interest must preferably be separated from the undesired signals. The signal present at the output of the differential high pass filter may also require an additional offset voltage [[6]] 65 and also may require resetting to a known initial condition or holding for noise rejection and/or sampling purposes [[7]] 66. It is also optionally possible that the high pass and low pass characteristic in some applications may require changing (in response, for example, to a control signal [[8]] 67).

Please amend paragraphs 0032-0036 as follows:

[0032] FIG. 1 shows a block diagram of the system with the feedback having the same units as the input, i.e. voltage or current. FIG. 1 further depicts the general concept of providing differential feedback 13 to an input stage 11 to alter the DC and/or low frequency state of the system. The loop feedback could be any suitable transfer function to accommodate the needs of a particular application.

[0033] FIG. 2 shows an embodiment comprising a practical continuous time implementation of the circuit suitable for discrete design. A high impedance input differential gain stage [[1]] 20 amplifies the input signal along with an error feedback parameter 27. This differential signal is converted to a single ended signal by a downstream module [[2]] 21. In this implementation, the gain is largely determined by resistor Rg [[8]] 22. This stage has a gain of 2*Rb/Rg for differential signals and a gain of 1 for common mode signals. This allows highly effective common mode performance to be achieved.

[0034] A second stage [[2]] 21 differences the output of the first stage to cancel common mode signals and convert the differential input to a single ended output. The output of this second stage [[2]] 21 is fed through a hold switch [[3]] 23 to an optional low pass filter [[4]] 24. The advantage of including this filter in the loop is that the loop will cancel offset voltages of the filter. This filter can be included to create a band pass response to the system as well as serving as an anti-aliasing filter.

[0035] The output of stage 23 or 24 ~~2 or 4~~ is then fed through a hold switch [[3]] 29 through one of a number of possible resistors [[5]] 31 to introduce various resistor dependant currents into the integrator [[6]] 26. By selecting various resistors at this point, differing high pass cutoff

frequencies can be achieved. The output of the integrator [[6]] 26 is converted to a differential current by a transconductance amplifier [[7]] 27. This amplifier will preferably present high drain impedances to connection points A and B in order to maintain high common mode rejection. It will be appreciated that the error current introduced across resistor Rg effectively cancels DC or low frequency signals present at IN+ and IN- represented by the voltage source [[9]].

[0036] Vb1 can be set to a voltage that represents the best output voltage of the integrator to attain an optimal error signal. One example would be to keep the operational transconductance amplifier [[7]] 27 in the saturation region. The overall DC offset present in the output signal is set by Vb2 making this voltage a suitable point to introduce an offset in a digital sampled system using a single ended supply. Input impedance of this implementation is preferably kept very high due to the input stage construction. It will of course be appreciated that this circuit could be constructed in single ended or differential form.

Please amend paragraphs 0038 through 0042 as follows:

[0038] Resetting of the high pass filter can be achieved by speeding up the clock rate of clock o3 25 (see FIG. 3) to move the pole away from the imaginary axis. This circuit can be implemented to achieve a very low supply current/performance ratio.

[0039] In FIGS. 2 and 3, an attenuator [[12]] 31 can be included to reduce the overall feedback gain to thereby allow potentially more practical values of integrating components. For example, the effective resistance of switch [[3,5]] 23, 25 of FIG. 3 can be set very high (higher than is practical in a silicon implementation) allowing more practical implementation.

[0040] FIG. 5A presents a relatively simple embodiment. Here the input signal is differentiated directly via a charge present on capacitor C1. As the input is being sampled, the feedback required to drive the error to zero is sampled by capacitor C2. When the switches are toggled, the error voltage is added to the input to zero the error voltage. The high pass cutoff frequency as well as transient blanking can be controlled with switch SW1.

[0041] FIG. 5B show a similar circuit utilizing a charge amplifier. The first stage has a negative gain, which is accounted for by introducing a phase reversal in the switches [[2]] 52. Transient blanking can be controlled by switch [[3]] 53 as well as the cutoff frequency.

[0042] In both discrete and integrated designs, various methods can be used to achieve the desired results. FIGS. 2 and 3 depict embodiments realized in discrete components. FIG. 4 presents a MOSFET embodiment. In an integrated form as shown in FIGS. 4a and 4b, a differential operational transconductance amplifier feeds back error currents to the input stages of a differential amplifier. The current can be fed back to any stage suitable for error differencing. In FIG. 4b, the error current is fed back to points [[1]] 41 and [[2]] 42 causing a balancing effect in the early stages. With a phase reversal as indicated on the drawing the current can be fed back to points [[3]] 43 and [[4]] 44. The differences between these two are subtle and relate to overall frequency stability and bias point considerations.